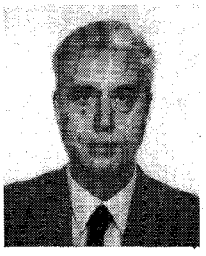

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A Novel *K*-Band Balanced FET Up-Converter

TETSUO HIROTA AND HIROYO OGAWA

Abstract—**The performance of the *K*-band balanced FET up-converter is described. A novel circuit configuration effective in enhancing conversion gain in the FET up-converter is proposed. An analysis using a simplified circuit model shows the effect of LO feedback in the balanced circuit. A conversion gain of 0.9 dB was experimentally obtained at 20 GHz. Maximum output power was 15.9 dBm.**

I. Introduction

GREAT PROGRESS has been made in the GaAs FET from microwave to millimeter-wave frequency ranges. Up until now, high-power and low-noise amplifiers have been developed using FET's. Recently, GaAs FET's are not only being applied to amplifiers, but also to various nonlinear functional circuits, such as frequency converters [1]–[4] and frequency doublers [5]–[7]. The advantages FET's offer are 1) excellent input–output isolation, and 2) desirable output power and gain capability.

The GaAs FET up-converters reported so far have achieved a 0-dB conversion gain at 6 GHz [3] and 8 GHz [4]. The performance of these FET up-converters, however, becomes degraded at *K*-band or higher frequencies due to various parasitic reactance effects.

In this paper, a novel approach to enhance the conversion gain of FET up-converters is proposed. The fundamental characteristics of the FET up-converter are described in Section II. Then, loss-reduction effect gained by LO load optimization is discussed in Section III. The performance of the balanced FET up-converter is presented in Section IV.

II. Frequency Conversion in FET's

Fundamental frequency conversion characteristics of FET's have been experimentally investigated in *K*-band. This investigation includes an examination of the optimum impedance matching conditions and bias points for up-converters. The circuit configuration for an experiment applies both LO power and IF input signal to the gate of source-grounded FET's as shown in Fig. 1. LO and IF signals are mixed by the nonlinear relationship of gate-voltage to drain-current, and the up-converted signal is obtained from the drain. Another approach is to use a dual-gate FET. For up-converter applications, however, a single-gate FET is preferable because it excels in high-frequency performance and the separation of LO and IF is

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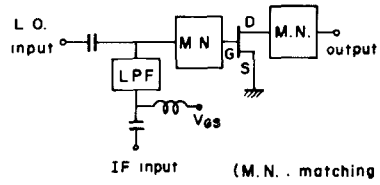

Fig. 1. Circuit configuration of single-ended up-converter.

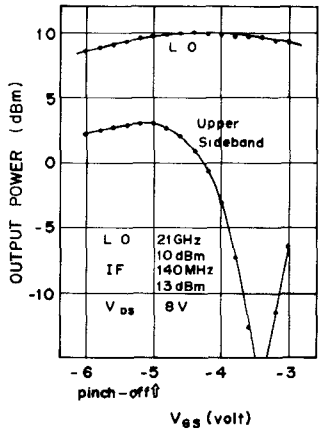

Fig. 2. Output power dependence on gate-bias voltage V_{GS}.

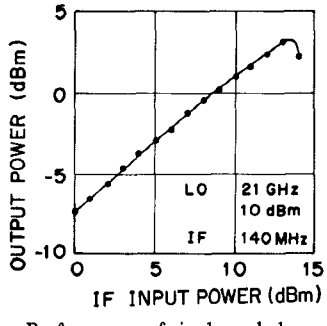

Fig. 3. Performance of single-ended up-converter.

not a difficult matter. The FET used in these experiments has a 0.5-μm gate length, 750-μm gate width, and an I_{DSS} of 220–240 mA. An alumina ceramic substrate of 0.3 mm in thickness and an FET chip are soldered to a metal mount.

Output power versus gate-bias voltage in the FET up-converter is shown in Fig. 2. The output signal reaches maximum at pinch-off voltage, where the input signals are clipped. The LO level at the output port is as high as that at the input port. IF to RF conversion characteristics under the optimum dc-bias condition near pinch-off is shown in Fig. 3. Conversion loss from LO to output signal (upper sideband) is 7 dB when saturated with input IF signal. This value is 10 dB lower than the output power of the FET used as an amplifier. The experimental results are consistent with those conducted at 6 GHz [3] and will be explained through the analysis introduced in Section III. In this circuit configuration, conversion loss is fairly large at the high-frequency region where FET gain is not sufficiently high.

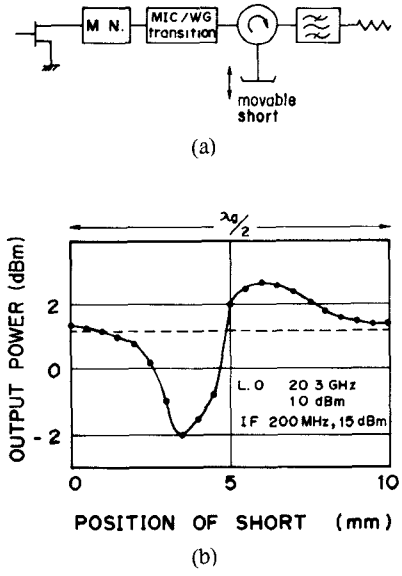

Fig. 4. Effect of LO reflection at the output. (a) Experimental setup. (b) Measured up-converted signal power.

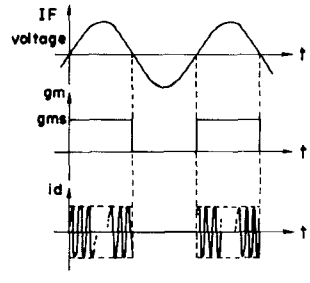

Fig. 5. Simplified operation model with a large IF power.

III. Effect of LO Reflection

A. Experimental Investigation

In the single-ended circuit shown in Fig. 1, the input port is matched to LO and the output port is matched to both signal output and LO. The performance of the FET is strongly dependent on load conditions, as reported in regard to frequency doublers [6] [7]. It is expected that up-converter performance can be improved by optimizing the load for high-level LO output.

An experiment was performed using the setup shown in Fig. 4(a). The upper sideband signal passes through the filter located at the load circuit, while the LO signal is reflected and fed back into the FET through a circulator and sliding short. The data measured is given in Fig. 4(b). LO reflection in the appropriate phase results in lower conversion loss compared with that of matched termination, which is indicated by a broken line in Fig. 5(b). Though the results are affected by circuit losses in the microstrip-to-waveguide transition, the circulator and in the bandpass filter, a conversion-loss reduction can be clearly seen.

B. Analysis

The experimental results given in Sections II and III-A can be explained through the following simplified model.

Since the input impedance for IF frequency is high, the gate voltage swing of the IF signal is considerably large. Therefore, FET transconductance $g_m(t)$ can be approximated by its saturation value g_{ms} at positive half cycles of the IF signal and zero at negative half cycles, as shown in Fig. 5. $g_m(t)$ is expanded by Fourier series as follows:

$$g_m(t) = g_{ms}\left(\frac{1}{2} + \frac{2}{\pi}\sin\omega_s t + \cdots\right) \tag{1}$$

where ω_s is the IF frequency. When the LO voltage of a frequency ω_p and an amplitude a is applied, drain current i_d is expressed as

$$\begin{aligned} i_d(t) &= g_m(t)\cdot a\sin\omega_p t \\ &= g_{ms}\cdot a\cdot\left[\frac{1}{2}\sin\omega_p t - \frac{1}{\pi}\{\cos(\omega_p+\omega_s)t \right. \\ &\quad \left. -\cos(\omega_p-\omega_s)t\} + \cdots\right]. \end{aligned} \tag{2}$$

This means that the signal output is lower by the factor of $1/\pi$ (-9.9 dB) than the maximum output of the FET used as an amplifier.

In Section III-A, it was experimentally shown that the conversion loss should be reduced by the LO signal reflection at the output circuit. The factors which can produce this effect are 1) $I_{DS}-V_{DS}$ nonlinearity and 2) internal feedback through gate–drain capacitance C_{gd} or source inductance. The former is considered to have a small effect, as can be seen in dc characteristics. On the other hand, the gate–drain impedance $1/\omega C_{gd}$ drops to about 100 Ω at K-band, which may cause considerable feedback effect.

Loss reduction is evaluated using the circuit model shown in Fig. 6, where jX and jB represent gate–source and gate–drain capacitance, respectively. The voltage applied to jX includes the components of upper sideband $\omega_u(=\omega_p+\omega_s)$, lower sideband $\omega_l(=\omega_p-\omega_s)$ in addition to LO (ω_p). If higher order terms are neglected in (2), drain current i_d and gate voltage v_g are expressed as

$$\begin{aligned} id &= \mathrm{Re}\left\{I_p e^{j\omega_p t} + I_u e^{j\omega_u t} + I_l e^{j\omega_l t}\right\} \\ v_g &= \mathrm{Re}\left\{V_p e^{j\omega_p t} + V_u e^{j\omega_u t} + V_l e^{j\omega_l t}\right\} \end{aligned} \tag{3}$$

where suffixes u, l, p stand for the components of the frequencies $\omega_u, \omega_l, \omega_p$, respectively. Also, I_p, I_u, and I_l are related to V_p, V_u, and V_l as follows:

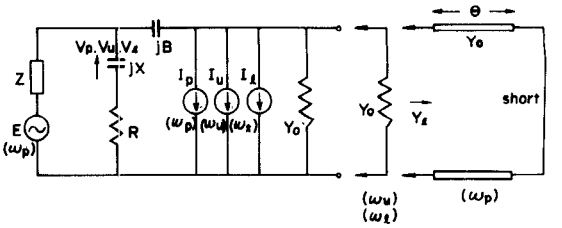

Fig. 6. Circuit model for analysis.

$$\begin{bmatrix} I_p \\ I_u \\ I_l \end{bmatrix} = g_{ms}\begin{bmatrix} \frac{1}{2} & \frac{j}{\pi} & -\frac{j}{\pi} \\ -\frac{j}{\pi} & \frac{1}{2} & 0 \\ \frac{j}{\pi} & 0 & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_p \\ V_u \\ V_l \end{bmatrix}. \tag{4}$$

The load is a reactive circuit for ω_p represented by the admittance Y_l, and Y_0 for other frequencies. The value of jX and jB can be assumed frequency-independent when ω_u and ω_l are close to ω_p. The voltages V_p, V_u, V_l excited by current sources I_p, I_u, I_l and input source $\mathscr{E}$ are written as follows:

$$\begin{bmatrix} V_p \\ V_u \\ V_l \end{bmatrix} = \begin{bmatrix} A_2 & 0 & 0 & A_3 \\ 0 & A_1 & 0 & 0 \\ 0 & 0 & A_1 & 0 \end{bmatrix}\begin{bmatrix} I_p \\ I_u \\ I_l \\ \mathscr{E} \end{bmatrix} \tag{5}$$

where

$$\begin{cases} A_1 = XB/\left[2Y_0 + jB + j2BY_0(R-jX) + \frac{1}{Z}(2Y_0+jB)(R+jX)\right] \\ A_2 = XB/\left[Y_0 + Y_l + jB + jB(Y_0+Y_l)(R+jX) + \frac{1}{Z}(Y_0+Y_l+jB)(R+jX)\right] \\ A_3 = j\frac{X}{Z}(Y_0+Y_l+jB)/\left[Y_0+Y_l+jB(Y_0+Y_l)(R+jX) + \frac{1}{Z}(Y_-+Y_l+jB)(R+jX)\right] \\ Y_l = -jY_0\cot\theta. \end{cases}$$

Eliminating, V_p, V_u, V_l from (4) and (5), we have

$$\begin{aligned} \begin{bmatrix} I_p \\ I_u \\ I_l \end{bmatrix} &= g_{ms}\begin{bmatrix} \frac{1}{2} & \frac{j}{\pi} & -\frac{j}{\pi} \\ -\frac{j}{\pi} & \frac{1}{2} & 0 \\ \frac{j}{\pi} & 0 & \frac{1}{2} \end{bmatrix}\begin{bmatrix} A_2 & 0 & 0 & A_3 \\ 0 & A_1 & 0 & 0 \\ 0 & 0 & A_1 & 0 \end{bmatrix}\begin{bmatrix} I_p \\ I_u \\ I_l \\ \mathscr{E} \end{bmatrix} \\ &= g_{ms}\begin{bmatrix} \frac{1}{2}A_2 & \frac{j}{\pi}A_1 & -\frac{j}{\pi}A_1 \\ -\frac{j}{\pi}A_2 & \frac{1}{2}A_1 & 0 \\ \frac{j}{\pi}A_2 & 0 & \frac{1}{2}A_1 \end{bmatrix}\begin{bmatrix} I_p \\ I_u \\ I_l \end{bmatrix} + g_{ms}A_3\mathscr{E}\begin{bmatrix} \frac{1}{2} \\ -\frac{j}{\pi} \\ \frac{j}{\pi} \end{bmatrix}. \end{aligned} \tag{6}$$

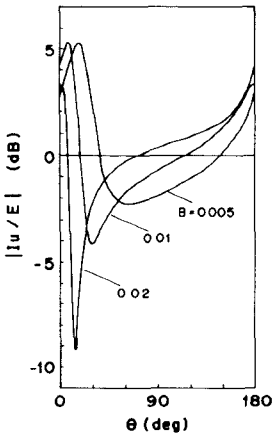

Fig. 7. Relative conversion gain as a function of LO reflection angle θ.

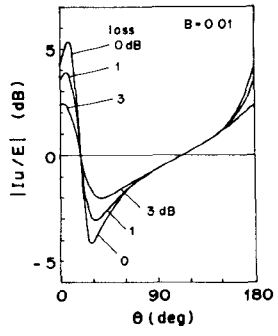

Fig. 8. Relative conversion gain with a lossy reflection circuit for LO.

Upper-sideband current I_u is calculated from the next equation:

$$\begin{bmatrix} \frac{1}{g_{ms}} - \frac{1}{2}A_2 & -\frac{j}{\pi}A_1 & \frac{j}{\pi}A_1 \\ \frac{j}{\pi}A_2 & \frac{1}{g_{ms}} - \frac{1}{2}A_1 & 0 \\ -\frac{j}{\pi}A_2 & 0 & \frac{1}{g_{ms}} - \frac{1}{2}A_1 \end{bmatrix} \begin{bmatrix} I_p \\ I_u \\ I_l \end{bmatrix} = A_3 \mathscr{E} \begin{bmatrix} \frac{1}{2} \\ -\frac{j}{\pi} \\ \frac{j}{\pi} \end{bmatrix}. \quad (7)$$

Results are shown in Fig. 7. The conversion-loss reduction is plotted against reflection angle θ. The line of 0 dB corresponds to $Y_l = Y_0$. Parameters used in the calculation are:

$$Y_0 = 0.05(\sigma), \qquad R = 1(\Omega), \qquad X = -10(\Omega),$$
$$Z = R - jX$$
$$g_{ms} = g_{ms0} \cdot e^{-j\omega\tau}, \qquad g_{ms0} = 0.05(\sigma),$$
$$\omega\tau = 0_1 2\pi$$
$$B = 0.005 \sim 0.02(\sigma).$$

These values are typical for the FET with a 0.5 μm$\times$ 750 μm gate in the K-band. A direct comparison with Fig. 4(b) is difficult, because of the phase rotation in the bonding wires and matching network. However, loss-reduction effect can be found, as it also was in the experiment. It is now seen that the main factor in loss-reduction is internal feedback through C_{gd}. The LO reflection is less effective when the circuit for reflection is lossy, as shown in Fig. 8.

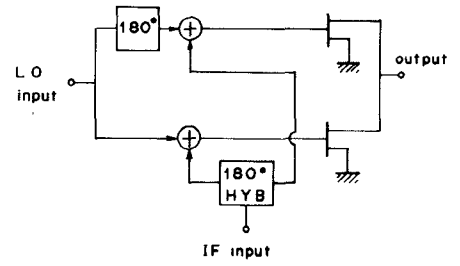

Fig. 9. Configuration of balanced up-converter.

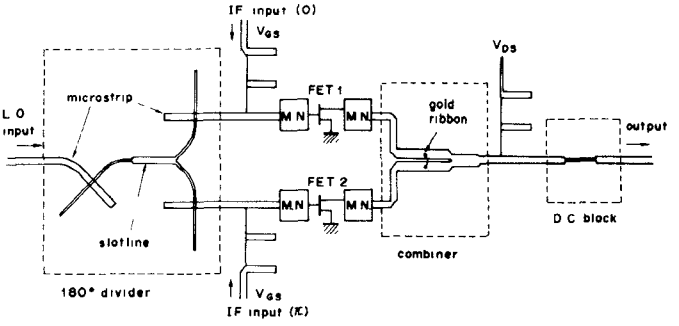

Fig. 10. Layout of balanced up-converter.

IV. Balanced Up-Converter

A. Circuit Configuration

It is not easy to realize the load circuit, which is reactive for ω_p and matched for ω_u on low-Q MIC, because ω_p is close to ω_u. The balanced configuration shown in Fig. 9 provides a good means for solving this problem. The LO signals 180° out-of-phase are mixed with IF signals fed from a 180° hybrid. The output signals at ω_u are in-phase and the LO signals are out-of-phase. Therefore, the combining point is a virtual ground for ω_p, providing a reactive load. This circuit needs no circulators or filters, and is, therefore, suited for MIC.

The layout of the 20-GHz balanced up-converter is shown in Fig. 10. A 180° phase difference between the LO signals is obtained through the slotline Y-junction formed on the other side of the substrate, and this junction also works as a blocking circuit for dc and IF signals. The combining circuit must have tuning capability because optimum combining position is difficult to predict. The combiner used here consists of a coupled microstrip with an even-mode characteristic impedance of 50 Ω, and a gold ribbon connecting the coupled lines. The optimum LO reflection phase can be obtained by adjusting the position of the gold ribbon. The influence of the ribbon on up-con-

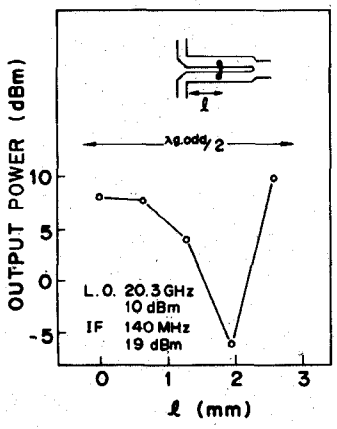

Fig. 11. Up-converted output power as a function of gold ribbon position.

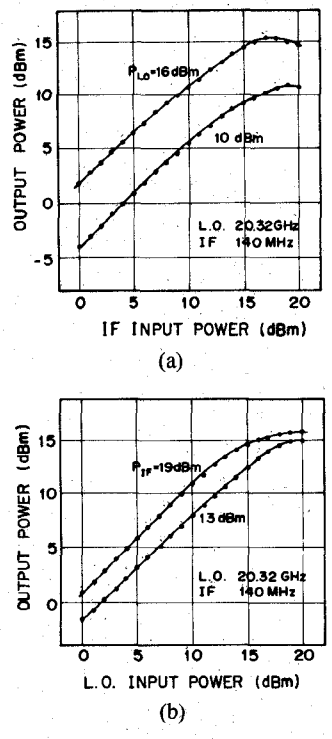

Fig. 12. Performance of 20 GHz balanced FET up-converter. (a) Output power as a function of IF input power. (b) Output power as a function of LO input power.

verted signal is small, because the up-converted signal propagates on a coupled line in even mode.

B. Experimental Results

The measured output power of the up-converted signal versus the position of gold ribbon is shown in Fig. 11. The dependence on load for LO is so strong that there is a high power variation of 15 dB. The performance of the up-converter with the adjusted ribbon position is shown in Fig. 12. The 20-GHz output power is plotted in Fig. 12(a) as a function of 140 MHz (IF) input power. The converter has a conversion gain of 0.9 dB from the 10 dBm LO to up-converted signal. The output power varies with LO power as shown in Fig. 12(b). Maximum output power is 15.9 dBm. The LO level measured at the output port is 12 dB lower than the up-converted output power without an external filter.

V. Conclusions

A balanced configuration for the FET up-converter has been proposed. The circuit employs a slotline Y-junction as a 180° divider, and a coupled-microstrip tunable combiner. In the balanced up-converter, the LO signals are fed back to the FET's, and conversion loss can be greatly reduced by the FET internal feedback effect.

A balanced up-converter has been fabricated at 20-GHz band. A conversion gain of 0.9 dB from LO to up-converted signal and maximum output power of 15.9 dBm are achieved in up-converter performance.

FET up-converter is effective to realize a compact FET transmitter with a high performance at the millimeter-wave band.

Acknowledgment

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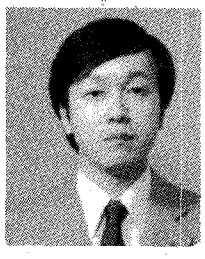

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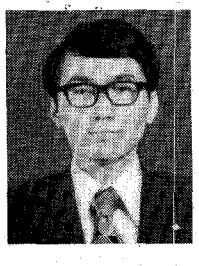

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